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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,988	04/28/2005	Hiromi Ebara	2005-0683A	3027
513 7590 09/04/2007 WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021			EXAMINER LOONAN, ERIC T	
			ART UNIT 2189	PAPER NUMBER
			MAIL DATE 09/04/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/532,988	Applicant(s) EBARA ET AL.	
	Examiner Eric Loonan	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 April 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>28 April 2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is the initial Office action based on the 10/532988 application filed 28 April 2005. Claims 1-16, as originally filed, are currently pending and have been considered below.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 28 April 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.
2. Document WO-00/51087 has been considered with regards to the English translation of the abstract only. Document JP-2001-14441 has been considered with respect to Document WO 00/65602 and with respect to the cited explanation of relevance in the background art section of the applicant's specification. Document JP-2001-188701 has been considered with respect to WO 01/29670. The remaining documents have been fully considered.

Specification

3. The disclosure is objected to because of the following informalities: Several spelling and grammatical errors exist in the specification. Some examples include:
 - Page 1, Line 17: "heavy attentions"
 - Page 1, Lines 20-21: "and a connector" ... "SD memory card via the connector"

- Page 4, Line 14: "more than one programs access to the semiconductor memory"
- Page 13, Lines 17-22: "kind of EC applications" ... "kind of EC services"
- Page 24, Line 1: "In the indirections"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-3, 6-14, and 16** are rejected under 35 U.S.C. 102(e) as being anticipated by Nagamasa et al (US PGPub 2004/0177215) hereinafter known as Nagamasa.

Claim 1: Nagamasa teaches a semiconductor memory card comprising a tamper resistant module (Fig 1, 150 – IC Card Chip and 120 – Controller Chip) and a nonvolatile memory (Fig 1, 130 – Flash memory chip), wherein the tamper resistant module includes: an internal memory having a usage area used by a program stored in the tamper resistant module (Fig 26, 162 – EEPROM; Section [0043]); and a processing unit (Fig 26, 120 – Controller Chip) operable to (i) assign an area in the nonvolatile

memory to the program (Section [0051]), and (ii) generate, on the internal memory of the tamper resistant module, access information for the assigned area, the usage area and the assigned area thereby composing a total area for use by the program (Section [0055]).

Claim 2: Nagamasa teaches a semiconductor memory card wherein the internal memory stores a first area table indicating a location and a size of the usage area, and a second area table indicating a location and a size of the assigned area, and the access information is the second area table (Section [0051], Section [0052], Fig 21).

Claim 3: Nagamasa teaches a semiconductor memory card wherein the processing unit comprises: an assigning unit operable to assign, at a time of the generation of the access information, an encryption key which the program uses in accessing the assigned area (Fig 23, 2321 – User Certificate; Section [0055]); an encrypting unit operable, at a time of the program writing data to the assigned area, to encrypt the data (Fig 23, 2313; Section [0055]); and a decrypting unit operable, at a time of the program reading data from the assigned area, to decrypt the data (Fig 23 – 2324; Section [0055]).

Claim 6: Nagamasa teaches a semiconductor memory card wherein the nonvolatile memory includes a first memory module (Fig 1, 130 – Flash memory chip) and a second memory module (Fig 26, 160 – RAM), a unit of writing in the second memory module being smaller than a unit of writing in the first memory module, and the second memory module storing file management data (Section [0043]).

Claim 8: Nagamasa teaches a semiconductor memory card wherein the internal memory of the tamper resistant module includes a first memory module (Fig 26, 162 - EEPROM) and a second memory module (Fig 26, 160 – RAM), a unit of writing in the second memory module being smaller than a unit of writing in the first memory module, and the second memory module storing file management data (Section [0043]).

Claims 7 and 9: Nagamasa teaches a semiconductor memory card wherein the second memory module is one of a Ferroelectric Random Access Memory and a Magnetoresistive Random Access Memory (Fig 26, 160 – RAM).

Claim 10: Nagamasa teaches a semiconductor memory card being a multi-application memory card, wherein the program is one of applications with which the memory card is compatible, and the internal memory has a plurality of usage areas corresponding one to one to the applications (Fig 21, multiple areas are assigned to different processes; Section [0051]).

Claim 11: Nagamasa teaches a semiconductor memory card wherein at a time of addition of an application to the memory card, the processing unit assigns an area to be used by the added application (Fig 21, multiple areas are assigned to different processes; Section [0051]).

Claim 12: Nagamasa teaches a semiconductor memory card wherein the assigned area is a file system in which files are stored (Fig 21, 2130 – User File Area).

Claim 13: Nagamasa teaches a semiconductor memory card wherein the tamper resistant module includes a CPU that executes the program (Fig 1, 121 – CPU).

Claim 14: Nagamasa teaches a semiconductor memory card including a host interface which is an interface with a device connected to the memory card, wherein the host interface judges whether a command from the device is an expansion command, and the program starts, if the command is judged to be the expansion command (Section [0059]; DIO terminal 2544).

Claim 16: Nagamasa teaches a controlling program in a semiconductor memory card that comprises a tamper resistant module (Fig 1, 150 – IC Card Chip and 120 – Controller Chip) and a nonvolatile memory (Fig 1, 130 – Flash memory chip), and that is executed by a CPU in the tamper resistant module, wherein the tamper resistant module includes an internal memory having a usage area used by an application stored in the tamper resistant module (Fig 26, 162 – EEPROM; Section [0043]), and the controlling program is operable to (i) assign an area in the nonvolatile memory to the application (Section [0051]), and (ii) generate, on the internal memory of the tamper resistant module, access information for the assigned area, the usage area and the assigned area thereby composing a total area for use by the application (Section [0055]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagamasa in view of Madoukh (US PGPub 2001/0019614).

In **Claim 4**, Nagamasa discloses the semiconductor card of its parent claim.

In **Claim 5**, Nagamasa discloses the semiconductor card of its parent claim.

Further, Nagamasa teaches semiconductor memory card wherein the internal memory stores a first area table indicating a location and a size of the usage area, the nonvolatile memory stores a second area table indicating a location and a size of the assigned area (Section [0051], Section [0052], Fig 21).

In **Claim 4**, Nagamasa does not appear to explicitly disclose a semiconductor memory card wherein the processing unit further comprises: a receiving unit operable to receive a security level from the program; and a storage unit that stores values for different security levels, bit lengths of an encryption key, and encryption methods, the bit lengths and encryption methods corresponding one-to-one to the values, the encryption key assigned by the assigning unit is generated based on a bit length corresponding to the received security level, and the encryption and decryption by the encrypting unit and decrypting unit, respectively, are performed based on an encryption method corresponding to the received security level.

In **Claim 5**, Nagamasa does not appear to explicitly disclose a semiconductor memory card wherein the second area table being encrypted using a predetermined encryption key, and the access information is a set of the predetermined encryption key and information indicating a location of the second area table.

However, with respect to **Claim 4**, Madoukh teaches a receiving unit operable to receive a security level from the program; and a storage unit that stores values for different security levels (Section [0056]), bit lengths of an encryption key (Section [0044], keys with extended lengths), and encryption methods (Section [0044], different hashing algorithms), the bit lengths and encryption methods corresponding one-to-one to the values, the encryption key assigned by the assigning unit is generated based on a bit length corresponding to the received security level (Section [0045], encryption key manager assigns keys per the user session), and the encryption and decryption by the

encrypting unit and decrypting unit, respectively, are performed based on an encryption method corresponding to the received security level (Section [0044]).

However, with respect to **Claim 5**, Madoukh teaches an encryption key manager (Section [0045]).

Nagamasa and Madoukh are analogous art because they are from the same field of endeavor of data storage.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Nagamasa and Madoukh before him or her, to modify the semiconductor card of Nagamasa to include the encryption methods as taught by Madoukh.

The motivation for doing so would have been to deploy the data security methods onto the semiconductor card.

Therefore, it would have been obvious to combine Nagamasa with Madoukh to obtain the invention as specified in the instant claims.

8. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagamasa in view of Deo et al (US Patent 5,721,781) hereinafter known as Deo.

In **Claim 15**, Nagamasa discloses a semiconductor memory card that comprises a tamper resistant module and a nonvolatile memory, and includes a plurality of file systems.

Nagamasa does not appear to explicitly disclose a secure level of each of the file systems being one of high, medium, and low, wherein a first file system whose secure level is high is stored in the tamper resistant module, a second file system whose

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secure level is low is stored in the nonvolatile memory, and a third file system whose secure level is medium is stored in the nonvolatile memory, and access information for accessing the third file system is stored in the tamper resistant module.

However, Deo teaches an authentication system that utilizes different terminals for different security levels (Col 10, Lines 42-67).

Nagamasa and Deo are analogous art because they are from the same field of endeavor of semiconductor card transactions.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Nagamasa and Deo before him or her, to modify the semiconductor card of Nagamasa to include the authentication system as taught by Deo.

The motivation for doing so would have been to assign different security levels to data for the purpose of storing the data in different locations.

Therefore, it would have been obvious to combine Nagamasa with Deo to obtain the invention as specified in the instant claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Loonan whose telephone number is (571) 272-6994. The examiner can normally be reached on Monday-Friday, 7:30am-5:00pm EST.

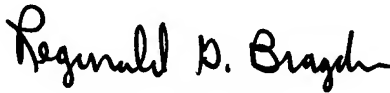
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ETL


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